What Is Claimed Is:

1. A program-controlled unit comprising a single controller core that has a first and at least a second execution unit (1, 2), which units are operable independently of one another in a first operating mode, and process the same instructions in parallel in a second operating mode.

2. The program-controlled unit as recited in Claim 1, wherein an error detection device (5, 6, 10, 11, 14) is provided that, in the second operating mode, performs an error detection and/or an error correction in accordance with an error handling routine.

3. The program-controlled unit as recited in Claim 2, wherein the error detection device (5, 6, 10', 11', 13', 14) has a coder (10', 11', 13') that equips input data conveyed to the execution units (1, 2) on the input side, and/or output signals calculated by a respective execution unit, with an error detection code and/or with an error correction code.

4. The program-controlled unit as recited in one of the Claims 2 or 3,
wherein the error detection device (5, 6, 10, 11, 14) contains a comparison unit (14), downstream from the two execution units on the output side, that compares the result data calculated by the execution units (1, 2) and/or their error correction codings, in accordance with an error handling routine, to determine the presence of errors, and outputs an error signal in the event an error is present.

5. The program-controlled unit as recited in one of the Claims 2 through 4,
wherein the error detection device (5, 6, 10, 11, 14) contains at least one second comparison unit, upstream

from at least one execution unit (1, 2) on the input side, that compares input data conveyed to a respective execution unit on the input side with the input data equipped with a checksum (e.g. parity, CRC, ECC), in accordance with an error detection routine, to determine the presence of an error, and outputs an error signal in the event an error is present.

6. The program-controlled unit as recited in one of the preceding claims,
wherein at least one data register (8, 9) is provided, which is associated with at least one of the execution units (1, 2) and is connected on the output side both to the inputs of the execution units (1, 2) and to the comparison unit (5, 6) upstream from the latter, and in which the input data for the execution units (1, 2) are storable.

7. The program-controlled unit as recited in one of the preceding claims,
wherein a shadow register is provided in which the input data most recently conveyed to the execution units (1, 2) prior to calculation in the execution units are stored.

8. The program-controlled unit as recited in Claim 7,
wherein the shadow register is embodied as a FIFO.

9. The program-controlled unit as recited in one of the preceding claims,
wherein a control device, coupled on the input side to the error detection device (5, 6, 10, 11, 14) and on the output side to the shadow register, is provided, which generates an enabling signal and thereby enables the shadow register only if no error is detected by the error detection device (5, 6, 10, 11, 14).

10. The program-controlled unit as recited in one of the preceding claims,

wherein the program-controlled unit is embodied as a microcontroller or microprocessor.

11. A method for operating a program-controlled unit as recited in one of the preceding claims, wherein the input data and/or the calculated result data and/or their error codings are compared with one another, and an error signal is generated if the result of the comparison does not agree.

12. The method as recited in Claim 11, wherein a separate error signal is outputted for each type of error.

13. The method as recited in one of the Claims 11 or 12, wherein the input data are first conveyed to both execution units (1, 2), and subsequently thereto the error correction code is created from the input data.

14. The method as recited in one of the Claims 11 through 13, wherein the stored input data of the last calculation are overwritten only if a comparison of those input data, or of the result data calculated from those input data, does not result in an error signal.

15. The method as recited in one of the Claims 11 through 14, wherein the result data are placed onto the bus only if an error signal is not present.